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(54) Interpolation pulse generating device

Vorrichtung zur Erzeugung von Interpolationspulsen

Dispositif pour générer des impulsions d'interpolation

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Description

[0001] The present invention relates to an interpolation pulse generating device for incorporation in a linear encoder, a rotary encoder, and like devices.

[0002] Length-measuring devices such as a linear encoder and a rotary encoder are known in which a detector generates sinusoidal signals having the same spatial period and a predetermined spatial phase difference in accordance with relative movement between stationary and moving scales, and pulses of a number corresponding to the distance of the above relative movement are generated on the basis of the sinusoidal signals (detection signals). Length-measuring devices of the above type are commonly used in three-dimensional measuring apparatuses, machine tools, small-sized digital slide calipers, etc.

[0003] Fig. 8 shows a linear encoder as an example of such length-measuring devices. This linear encoder consists of a scale 1, a detector 2 capable of sliding along the scale 1, an interpolation pulse generating device 3, and a positioning device 4. In actual implementation, the positioning device 4 is replaced by a counter or a NC positioning device including a counter of a three-dimensional measuring device or a NC machine tool. The detector 2 produces two cyclic detection signals (Vsinθ and Vcosθ in the example of Fig. 8) in accordance with relative movement between the scale 1 and the detector 2. Detecting a variation of the phase angle θ of the two detection signals, the interpolation pulse generating device 3 produces count-up pulses P_+ or count-down pulses P_-. The positioning device 4 recognizes the distance of the movement of the detector 2 relative to the scale 1 by counting the pulses P_+ or P_-.

[0004] Length-measuring devices of the above type are required to have a resolution that is higher than the resolution that is determined by the mechanical structure of the detector, which is the pitch of a grating formed on the scale in the case of a linear encoder. To this end, i.e., to improve the resolution of the length measurement, a phase angle variation of the detection signals that are output from the detector are detected in angular units that are smaller than one period, i.e., 2π. This operation is hereinafter called "interpolation."

[0005] In recent years, it is increasingly required that the interpolation be improved in accuracy and processing speed as the need of high-resolution length measurement is increased in the microprocessing technology. In particular, in such fields as semiconductors, length measurements in the order of nanometer or sub-nanometer, not to mention submicrometer, are needed increasingly.

[0006] Usually, in the interpolation of a phase angle variation of the above-described detection signals, computation is performed on a combination of a plurality of input signals that have the same period and amplitude, have a predetermined phase difference, and vary symmetrically with respect to the zero level. Conventionally, the resistive division scheme is mainly used for this computation.

[0007] The principle of the resistive division scheme will be described with reference to Fig. 9. When signals represented by Vsinθ and Vcosθ are respectively input to terminals A and B, a signal represented by

$$C = \{V(R_A^2 + R_B^2)^{1/2}/(R_A + R_B)\}\sin(\theta + \phi) \quad (1)$$

where

$$\phi = \tan^{-1}(R_A/R_B)$$

is output from terminal C. Therefore, a sine-wave signal that is advanced from the signal A by a predetermined phase angle φ can be obtained by properly determining resistances R_A and R_B.

[0008] A desired number of circuits having the above configuration are provided. Among those circuits, one having the output signal C that is closest to 0 is selected and its output signal C is detected. For example, to realize an interpolation number 80, 40 circuits are needed to provide sine-wave signals whose φ values range from 0 to π with intervals of 2π/80. That is, a large-sized circuit is needed which includes 40 comparators and 80 resistors. (Refer to Japanese Examined Patent Publication No. Sho. 62-33527.) Therefore, to increase the interpolation number in the resistive division scheme, the number of resistors and the circuit scale necessarily increase, to cause problems in the cost, size, power consumption, etc.

[0009] Japanese Examined Patent Publication No. Hei. 5-25285 discloses an improved version of the resistive division scheme, which consists of a coefficient storing element, a coefficient switching circuit, a multiplication-type D/A converter. According to this scheme, coefficients of cosφ and -sinφ with an arbitrary spatial phase φ are generated by use of the multiplication-type D/A converter. By performing a computation involving the above coefficients and the input signals Vsinθ and Vcosθ, a sine-wave signal that is delayed from the signal Vsinθ is obtained as follows:

$$V\sin\theta\cdot\cos\phi - V\cos\theta\cdot\sin\phi = V\sin(\theta - \phi) \quad (2)$$

[0010] The phase angle θ of the input signals can be detected by comparing the above computation result with the zero potential (i.e., a reference signal). However, to increase the interpolation number in this scheme, an expensive D/A converter of a large number of bits is needed, whose conversion speed is usually very slow. Due to the limitation of the slow conversion speed, the response speed of the interpolation pulse generating device is much reduced.

[0011] US-A-5218295 describes a system for processing fine position signals obtained from two magnetic sensors. The system produces sinusoidal wave signals different from each other by a quarter phase cycle. The system switches the phase so as to bring the pair of phase modulated signals in phase with each other and then calculates the weight constants for the pair of pulse with modulated signals. The pulse with modulated signals are then subjected to a weighted means by the use of determined weighted constants with the result that the disorder at the switching point is removed from the pulse with modulated signals.

[0012] EP-A-0543421 describes a fine positioning detection system which uses an AC output signal having a phase electrically shifted in accordance with the position of the moving object. A counted value of a counter circuit is sampled in response to an electrical phase change at a zero cross time point of the AC output signal. As a result of this the sampled counted value of the counter circuit represents the absolute position data of the moving object. A second absolute position detecting section generates one or more delayed clock signals that are delayed from a clock signal on the basis of which the counter circuit counts up by an amount of time smaller than one period of the clock signal. The system utilizes the one or more delayed clock signals to measure the zero cross time point of the AC output signal in accordance with a unit time smaller than the one period of the clock signal. The absolute position data is then output as the measured time point added to the sample counted values.

[0013] According to a first aspect of the invention, there is provided an interpolation pulse generating device that receives detection signals of a plurality of phases which signals are produced in accordance with a displacement of relative movement between corresponding members, and generates a count pulse for each predetermined phase angle pitch that is smaller than one period of the detection signals, comprising:

selecting means for generating signals S_j and S_{j-1} that are deviate from each other by a phase value of $2\pi/M$ by combining the plurality of detection signals, where M is a fixed integer;
difference signal generating means for generating a reference signal ΔS that represents a difference between the signals S_j and S_{j-1}; and
comparing means for generating an up-pulse or a down-pulse every time the signal S_j or S_{j-1} varies by $\Delta S/n$ where n is a fixed integer in a phase section of $2\pi/M$ in which one of the signals S_j and S_{j-1} has positive values and the other has negative values.

[0014] According to a second aspect of the present invention, there is provided an interpolation pulse generating device that receives detection signals of a plurality of phases which signals are produced in accordance with a displacement of relative movement between corresponding members, and generates a count pulse for each predetermined phase-angle pitch that is smaller than one period of the detection signals, comprising:

selecting means for receiving two sinusoidal detection signals that have the same amplitude, the same spatial period, and a predetermined spatial phase difference and that vary symmetrically with respect to a zero level, and for selecting, from M sinusoidal signals S_1-S_m deviating from each other at predetermined intervals, two adjacent sinusoidal signals S_j and S_{j-1} where an integer j = 1,2, ..., M, by combining the two sinusoidal detection signals;
difference signal generating means for generating a difference signal Δ_{sj} according to

$$\Delta_{sj} = S_{j-1} - S_j$$

and an inverted difference signal $-\Delta_{sj}$;
A/D-converting means for A/D-converting the sinusoidal signal S_{j-1} using the signals ΔS_j and $-\Delta S_j$ as references; and,
comparing means for comparing an output A of an n-ary counting means and an output B of the A/D converting means, and for outputting an up-pulse P_+ if the output A is smaller than or equal to the output B, and outputting a down-pulse P_- if the output A is larger than the output B;
the n-ary counting means for decrementing the integer k by 1 when receiving the down-pulse P_- and, in the event that a decremented result is smaller than 0, substituting n - 1 into k and outputting a borrow pulse, and for incrementing the integer k by 1 when receiving the up-pulse P_+ and, in the event that an incremented result is equal to

n, substituting 0 into k and outputting a carry pulse, a signal indicating the integer k being supplied to the comparing means as the output A; and

M-ary counting means for decrementing the integer j by 1 when receiving the borrow pulse and, in the event that a decremented result is equal to 0, substituting M into j, and for incrementing the integer j by 1 when receiving the carry pulse and, in the event that an incremented result is equal to M + 1, substituting 1 into j, a signal indicating the integer j being supplied to the selecting means.

[0015] The present invention provides, by using novel equations for computation, an interpolation pulse generating device which operates at high speed with high accuracy and resolution, and which has a smaller number of high-accuracy resistors and smaller high-speed circuits than the conventional device.

[0016] In the invention, the two kinds of interpolation means, i.e., the M-interpolation means and the n-interpolation means are provided to realize Mxn interpolation. A simple configuration can be obtained without using an unduly large number of resistors, comparators, etc. In a first embodiment, the n-interpolation is performed by using analog circuits. In a second embodiment, it is performed digitally by using an A/D converter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017]

Fig. 1 is a block diagram showing a general configuration of an interpolation pulse generating device according to an embodiment of the present invention;
Fig. 2 is a circuit diagram of an adjacent two phases selecting means used in the device of Fig. 1;
Fig. 3 is a circuit diagram of a difference signal generating means used in the device of Fig. 1;
Fig. 4 is a circuit diagram of a judgment signal generating means used in the device of Fig. 1;
Fig. 5 is a timing chart of respective signals in the device of Fig. 1;
Fig. 6 is a circuit diagram of a $k\Delta S_j/n$ generating means used in the device of Fig. 1;
Fig. 7 is a circuit diagram of first and second comparing means used in the device of Fig. 1;
Fig. 8 shows a general configuration of a linear encoder;
Fig. 9 shows the principle of the resistive division scheme;
Fig. 10 is a block diagram showing a general configuration of an interpolation pulse generating device according to a second embodiment of the invention;
Fig. 11 is a graph showing a relationship between an input signal and output data of an A/D converter used in the device of Fig. 10;
Fig. 12 is a circuit diagram of a damper circuit that may be used in the device of Fig. 10;
Fig. 13 is a timing chart showing the operation of the device of Fig. 10; and
Fig. 14 shows connection between a comparator and each of the A/D converter and an n-ary counting means, all of which are used in the device of Fig. 10.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0018] Preferred embodiments of the present invention will be hereinafter described with reference to the accompanying drawings.

[0019] Fig. 1 shows a circuit configuration of an interpolation pulse generating device according to an embodiment of the invention. An adjacent two phases selecting means 300 receives a detection signal 100 ($V\sin\theta$ in this embodiment) and a detection signal 200 ($V\cos\theta$ in this embodiment) that is always deviated from the detection signal 100 by a predetermined phase angle. Based on the detection signals 100 and 200, the adjacent two phases selecting means 300 divides one period 2π of the phase angle of the detection signals 100 and 200 into M parts, to produce two signals S_j and S_{j-1} ($j = 1, 2, ..., M$) that are deviated from each other by a phase angle of $2\pi/M$.

[0020] In this embodiment, the adjacent two phases selecting means includes means for generating sine-wave signals of M phases and means for selecting adjacent signals. Fig. 2 shows a preferred example of a circuit of the means 300. This circuit generates only one of the signals S_j and S_{j-1}, but a circuit for generating the other signal can be constructed in the same manner with an exception that the orders of resistors (described below) are shifted by one.

[0021] Referring to Fig. 2, the configuration and operation of the means 300 will be described.

[0022] The circuit of Fig. 2 consists of an inverting amplifier 303 receiving the detection signal 100, parallel-connected analog switching elements 304-1 to 304-M, resistors 305-1 to 305-M that are connected in series to the respective analog switching elements 304-1 to 304-M, an inverting amplifier 317 receiving the detection signal 200, parallel-connected analog switching elements 318-1 to 318-M, resistors 319-1 to 319-M that are connected in series to the respective analog switching elements 318-1 to 318-M, and inverting amplifiers 307 and 310. One of the resistors 305-1

to 305-M and one of the resistors 319-1 to 319-M (for instance, the resistors 304-1 and 318-1 or the resistors 304-2 and 318-2) are selected by the analog switching elements 304-1 to 304-M and 318-1 to 318-M in accordance with an output signal 80 of an M-ary counting means (M-ary reversible ring counter) 70. The selected resistors and the inverting amplifier 307 constitute a two-input addition type variable gain amplifier.

[0023] The resistances of the resistors 305-1 to 305-M are represented by R_{11} to R_{1M} and the resistances of the resistors 319-1 to 319-M are represented by R_{21} to R_{2M}. In accordance with the signal 80 supplied from the M-ary counting means 70 and indicating an integer j, analog switching elements 304-j and 318-j are turned on. In this state, an output signal of the inverting amplifier 307 is obtained as follows:

$$R \cdot V\sin\theta/R_{1j} + R \cdot V\cos\theta/R_{2j} \tag{3}$$

[0024] An output S_j of the inverting amplifier 310 is equal to an inverted sum of the output signal of the inverting amplifier 307 multiplied by 2, the output signal of the inverting amplifier 303 ($-V\sin\theta$), and the output signal of the inverting amplifier 317 ($-V\cos\theta$). That is,

$$S_j = V[\{1 - (2R/R_{1j})\}\sin\theta + \{1 - (2R/R_{2j})\}\cos\theta]$$

$$= V[\{1 - (2R/R_{1j})\}^2 + \{1 - (2R/R_{2j})\}^2]^{1/2}\sin(\theta + \phi) \tag{4}$$

where

$$\phi = \tan^{-1}\{(1 - 2R/R_{2j})/(1 - 2R/R_{1j})\}.$$

[0025] Therefore, one of M-phase signals having phase angle intervals of $2\pi/M$ can be selected by setting the resistances R_{11} to R_{1M} and R_{21} to R_{2M} so that ϕ values have intervals of $2\pi/M$, i.e., so that $(1 - 2R/R_{1j})$ in Equation (4) becomes equal to a coefficient $\cos(2\pi j/M)$ (j = 1, 2, ..., M) and $(1 - 2R/R_{2j})$ in Equation (4) becomes equal to a coefficient $-\sin(2\pi j/M)$ (j = 1, 2, ..., M). Further, the M-phase signals have the same amplitude as is understood from Equation (4), which includes a square root of a sum of $\cos^2$ and $\sin^2$. That is,

$$S_j = C_j\sin(\theta - 2\pi j/M) \tag{5}$$

where C_j represents the amplitude and j = 1, 2, ..., M.

[0026] A signal S_{j-1}, which is deviated from S_j by a phase angle of $2\pi/M$, is obtained by using the same configuration as shown in Fig. 2 with an exception that the orders of the resistors 305 and the resistors 319 are shifted by one and selecting among the analog switching elements 304 and 318 in accordance with the signal 80 that is supplied from the M-ary counting means 70. That is,

$$S_{j-1} = C_{j-1}\sin\{\theta - 2\pi(j - 1)/M\} \tag{6}$$

where C_{j-1} represents the amplitude and j = 1, 2, ..., M. When j = 1, S_{j-1} is made S_M.

[0027] It is noted that in Equations (5) and (6) a relationship $C_j = C_{j-1}$ holds.

[0028] Fig. 5 is a timing chart of the respective signals. For convenience of description, it is assumed that the input signals 100 and 200 have a spatial phase difference of 90°, that the phase angle θ representing the movement distance varies linearly, and that M = 8 and n = 4. It goes without saying that the invention is not limited to such a specific case. In parts (a) to (e) of Fig. 5, the vertical axes represent voltages and the horizontal axes represent the movement distance. As the phases of the signals 100 and 200 advance by $2\pi/8$ (see part (a) of Fig. 5), each of the signal S_{j-1} (see part (b) of Fig. 5) and the signal S_j (see part (c) of Fig. 5) forms a triangle in the vicinity of the zero level.

[0029] The signals S_{j-1} and S_j are input to a difference signal generating means 500 (see Fig. 3), which produces a difference signal $\Delta S_j/n$ according to Equation (7):

$$\Delta S_j/n = (S_{j-1} - S_j)/n \tag{7}$$

[0030] In Fig. 3, nR_0 and R_0 represent resistances and reference numeral 501 denotes an operational amplifier. As shown in part (d) of Fig. 5, the value of ΔS_j is almost constant.

[0031] The difference signal $\Delta S_j/n$ is input to a $k\Delta S_j/n$ generating means 600. Fig. 4 shows a specific circuit configuration of the means 600. Output signals 90 (9_1, 9_2, ..., 9_k, ..., 9_n) of an n-ary counting means (n-ary reversible ring counter) 60 are supplied to analog switching elements T_1, T_2, ..., T_k, ..., T_n as control signals for determining conduction/non-conduction thereof so that one of the switching elements T_1-T_n is made conductive and the other ones are made non-conductive. In Fig. 4, only the analog switching element T_k is in a conductive state. A resistor having a resistance (1/k)q is provided between the analog switching element T_k and an operational amplifier 601, which has a resistor having a resistance q. In this state, the operational amplifier 601 produces an output signal $-k\Delta S_j/n$.

[0032] The signals $-k\Delta S_j/n$ and S_{j-1} are input to a judgment signal generating means 700, which performs computation and produces a judgment signal S_x according to Equation (8):

$$\begin{aligned} S_x &= S_{j-1} - k\Delta S_j/n \\ &= S_{j-1} - (k/n)(S_{j-1} - S_j) \\ &= \{kS_j + (n - k)S_{j-1}\}/n \end{aligned} \tag{8}$$

[0033] Fig. 6 shows a specific circuit configuration of the judgment signal generating means 700. In Fig. 6, r_s denotes resistors, and numerals 701 and 702 denote operational amplifiers.

[0034] Referring to Fig. 1, the signal S_x is input to first and second comparing means 800 and 900. The first comparing means 800 compares S_x and 0, and the second comparing circuit 900 compares S_x and $\Delta S_j/n$.

[0035] Fig. 7 shows specific circuit configurations of the comparing means 800 and 900. In Fig. 7, reference numerals 801 and 901 denote comparators, and F/F1 and F/F2 denote flip-flops. The output of the flip-flop F/F1 or F/F2 changes from "0" to "1" at a rising edge of a 0-to-1 change of the output of the comparator 801 or 901 in response to a change of the signal S_x. The n-ary counting means 60 counts up or down at a rising edge of a 0-to-1 change of the output of the flip-flop F/F1 or F/F2. The analog switching elements T_1-T_n of the $k\Delta S_j/n$ generating means 600 are switched in accordance with the output signals 90 of the n-ary counting means 60. Further, by making the CL input of the flip-flop F/F1 or F/F2 negative with a certain delay by use of a delay element, the output thereof changes from "1" to "0." Thus, pulses P_+ and P_- can be generated. By providing a delay, spike noise can be neglected which occurs at switching of the analog switching elements T_1-T_n.

[0036] Referring to Fig. 1, now consider a case where the detection signals 100 and 200 vary in one direction, S_j and S_{j-1} vary accordingly, and thereby transition is made from a state of $S_x > 0$ to a state of $S_x < 0$. At this time, an output pulse P_- is obtained from the first comparing means 800. When the pulse P_- is input to the n-ary counting means 60, the analog switching elements T_1-T_n are switched in response to a transition of $k \rightarrow k\text{-}1$, so that a state of $S_x > 0$ is established. Where the detection signals 100 and 200 vary in the other direction, S_j and S_{j-1} vary accordingly, and thereby transition is made from a state of $S_x < \Delta S_j/n$ to a state of $S_x > \Delta S_j/n$. At this time, an output pulse P_+ is obtained from the second comparing means 900. When the pulse P_+ is input to the n-ary counting means 60, a state of $S_x < \Delta S_j/n$ is re-established in response to a transition of $k \rightarrow k+1$.

[0037] As the transition of $k \rightarrow k+1$ or $k \rightarrow k\text{-}1$ is repeated, a carry pulse 50 or a borrow pulse 51 is generated by the n-ary counting means 60 and input to the M-ary counting means 70, where a transition of $j \rightarrow j+1$ or $j \rightarrow j\text{-}1$ is effected. By constituting a feedback loop so as to change k and j in the above manner, S_x can always satisfy $S_x > 0$ and $S_x < \Delta S_j/n$.

[0038] Although in the above embodiment the feedback loop is so formed that the signal S_x always satisfy $S_x > 0$ and $S_x < \Delta S_j/n$, a feedback loop may be so formed that the signal S_x always satisfy $S_x < 0$ and $S_x > -\Delta S_j/n$.

[0039] Part (e) of Fig. 5 shows how S_x varies so as to satisfy $S_x > 0$ and $S_x < \Delta S_j/n$ while a pulse P_+ or P_- is generated. Since a sine wave is regarded as approximately straight in the vicinity of a phase 0°, the signal $\Delta S_j = S_{j-1} - Sj$ can be regarded as approximately constant in a phase range of $2\pi/M$ including 0° if the division number M is sufficiently large. Thus, ΔS_j or $\Delta S_j/n$ can be used as a reference signal for the comparison.

[0040] Next, an interpolation pulse generating device according to a second embodiment of the invention will be described. While in the above embodiment the division by n is an analog operation, in this embodiment it is performed digitally.

[0041] Fig. 10 shows the entire configuration of the interpolation pulse generating device of this embodiment. Since the M-ary counting means 70 and the adjacent two phases selecting means 300, which together perform the M-division operation, are the same as those in the above embodiment (see Fig. 1), the following description is dedicated to the digital n-division technique.

[0042] The signals S_j and S_{j-1} are supplied from the adjacent two phases selecting means 300 to a difference signal

generating means 520, which produces a signal ΔS_j and an inverted signal $-\Delta S_j$ according to Equation (9):

$$\Delta S_j = S_{j-1} - S_j \quad (9)$$

[0043] The signals ΔS_j and $-\Delta S_j$ are input to an A/D converter 1100 as positive and negative references, respectively. The A/D converter 1100 constitutes a bipolar A/D converter.

[0044] Fig. 11 shows a relationship between an input voltage and output data of the A/D converter 1100. For simplicity, only upper 4 bits of output data are shown in Fig. 11.

[0045] The output signal S_{j-1} of the adjacent two phases selecting means 300 is converted into a digital code by the A/D converter 1100 according to the relationship of Fig. 11. The digitized signal S_{j-1} is input to a comparing circuit 1200, where it is compared with the value of a signal supplied from an n-ary counting means 61. Now the inputs from the n-ary counting means 61 and the A/D converter 1100 are represented by A and B, respectively. The comparing circuit 1200 makes the A>B output "true" when A > B, and makes the A≤B output "true" when A ≤ B. The A>B output and the A≤B output are ANDed with a timing signal 1310 from a timing generating circuit 1300, so that a pulse P_+ or P_- is produced.

[0046] The n-ary counting means 61 is constituted of an up/down reversible counter. When receiving a pulse P_+ from the comparing circuit 1200, the n-ary counting means 61 changes its count value from k to k+1. The input A of the comparator 1210 is updated accordingly, and compared with the input B at the next timing. When receiving a pulse P_- from the comparing circuit 1200, the n-ary counting means 61 changes its count value from k to k-1.

[0047] As the transition of $k \rightarrow k+1$ or $k \rightarrow k-1$ is repeated, a carry pulse 50 or a borrow pulse 51 is generated and input to the M-ary counting means 70. As a result, the M-ary counting means 70 changes its count value j to j+1 or j-1. By constituting a feedback loop so as to change k and j in the above manner, the count pulses P_+ and P_- can be generated so as to follow the phase angle variations of the detection signals 100 and 200.

[0048] It is noted that unnecessary count pulses P_+ and P_- are always generated alternately even if no change occurs in the detection signals 100 and 200. This phenomenon can be prevented by adding a damper circuit as shown in Fig. 12. That is, the damper circuit outputs a count-up or count-down pulse only when pulses P_+ or P_- are produced consecutively.

[0049] Next, the respective components shown in Fig. 10 will be described with an assumption that the division value n of the n-ary counting means 61 is 4. Further, as mentioned above,

[0050] Fig. 11 shows only upper 4 bits of output data of the A/D converter 1100 and plots a straight line, though actually the output data are discrete. Since n is equal to 4, it is assumed that the n-ary counting means 61 is constituted of a 2-bit binary reversible counter. It is also assumed that the A/D converter 1100 and the comparator 1210 deal with x+1-bit data.

[0051] Fig. 14 shows how each of the A/D converter 1100 and the n-ary counting means 61 is connected to the comparator 1210. The bits of the A/D converter 1100 and those of the comparator 1210 (B input bits) are in one-to-one correspondence. As for the input terminals (A input bits) of the comparator 1210 for the n-ary counting means 61, the 2^x bit is always set "true" (has a value "1"), the 2^{x-1} bit and the 2^{x-2} bit are allocated to the 2-bit input from the n-ary counting means 61, and the remaining lower bits are always set "false" (has a value "0").

[0052] The operation of the interpolation pulse generating device will be described with reference to Fig. 13. It is assumed that at first the signal S_{j-1} as digitized by the A/D converter 1100 is $(1000)\ldots)_2$, i.e., 0 V, and the count value k of the n-ary counting means 61 is $(00)_2$, and that the phase angles of the detection signals 100 and 200 vary at a constant rate. In this case, as indicated by symbol B in Fig. 13, the output of the A/D converter 1100, i.e., the input B of the comparing circuit 1200 increases with an approximately constant slope in a phase section of $2\pi/M$.

[0053] The comparing circuit 1200 compares the input B with the input A, i.e., the output of the n-ary counting means 61 in synchronism with the timing signal 1310 that is supplied from the pulse generating circuit 1300.

[0054] At the first timing, since A < B, a pulse P_+ is produced and the count value of the n-ary counting means 61 changes from $(00)_2$ to $(01)_2$. At the second timing, since A > B, a pulse P_- is produced and the count value of the n-ary counting means 61 changes from $(01)_2$ to $(00)_2$. In this manner, the comparing circuit 1200 outputs a pulse P_+ or P_- based on the result of comparison between the output values of the A/D converter 1100 and the n-ary counting means 61.

[0055] At the 20th, 22nd or 24th timing, the count value of the n-ary counting means 61 changes from $(11)_2$ to $(00)_2$. At this time, the n-ary counting means 61 produces a carry pulse 50, so that the count value of the M-ary counting means 70 changes from j to j+1. At the 21st or 23rd timing, the count value of the n-ary counting means 61 changes from $(00)_2$ to $(11)_2$. At this time, the n-ary counting means 61 produces a borrow pulse 51, so that the count value of the M-ary counting means 70 changes from j to j-1.

[0056] If the damper circuit of Fig. 12 is added as described above, alternately-output pulses P_+ and P_- do not take

effect. That is, a count-up or count-down pulse is output only when pulses P_+ or P_- are produced consecutively as at the 7th and 8th timings. It is understood that one period obtained by the M-division is further divided into 4 parts.

[0057] In this embodiment, n is assumed to be 4, and therefore the n-ary counting means 61 is implemented as a 2-bit binary reversible counter. Further, the 2^x bit of the A input bits of the comparator 1210 is always set "true" (has a value "1") and the output of the n-ary counting means 61 is supplied to the 2^{x-1} and 2^{x-2} bit terminals. The above embodiment can easily accommodate a case where n is larger than 4 by changing the connection for the input A of the comparator 1210 as long as n is a certain power of 2.

[0058] A description will now be made of why the reference signal is obtained by performing a computation on the input signals, i.e., detection signals Vsinθ and Vcosθ. It may be conceived to simply use a constant voltage generator or the like instead of the reference signal ΔS_j, which is approximately constant theoretically as shown in part (e) of Fig. 5. However, the amplitude V of the detection signals Vsinθ and Vcosθ that are output from the detector may vary due to a temperature variation or a variation in performance of the operational amplifiers. If the reference signal for comparison with the judgment signal S_x is so generated as to vary in proportion to the amplitude V of the signals S_j and S_{j-1} as in the case of ΔS_j in the above embodiment, the influence on the interpolation pitch error can greatly be reduced, which enables provision of an interpolation pulse generating device having high accuracy and resolution.

[0059] As described above, according to the invention, the interpolation is performed in two stages, i.e., M-division and n-division, and it is utilized that a sine wave can be regarded as approximately straight in the vicinity of a phase 0°. Therefore, a simple, less expensive interpolation pulse generating device that operates at high speed and has high accuracy and resolution can be provided by using a smaller number of high-accuracy resistors and switching circuits of two stages (M and n).

Claims

1. An interpolation pulse generating device that receives detection signals of a plurality of phases which signals are produced in accordance with a displacement of relative movement between corresponding members, and generates a count pulse for each predetermined phase-angle pitch that is smaller than one period of the detection signals, comprising:

   selecting means (300) for generating signals S_j and S_{j-1} that deviate from each other by a phase value of $2\pi/M$ by combining the plurality of detection signals, where M is a fixed integer;
   difference signal generating means (500) for generating a reference signal ΔS that represents a difference between the signals S_j and S_{j-1}; and
   comparing means (800,900) for generating an up-pulse or a down-pulse every time the signal S_j or S_{j-1} varies by $\Delta S/n$ where n is a fixed integer in a phase section of $2\pi/M$ in which one of the signals S_j and S_{j-1} has positive values and the other has negative values.

2. The interpolation pulse generating device according to claim 1, wherein the selecting means (300) receives two sinusoidal detection signals that have the same amplitude, the same spatial period, and a predetermined spatial phase difference and that vary symmetrically with respect to a zero level, and wherein the selecting means selects signals S_j and S_{j-1} where an integer J = 1,2 ..., M, from M sinusoidal signals S_1-S_M which deviate from each other at predetermined intervals, by combining the two sinusoidal detection signals.

3. The interpolation pulse generating device according to claim 1 or claim 2, further comprising:

   n-ary counting means (60) for outputting a first count value and a carry or borrow pulse by counting the up-pulse and the down-pulse, the first count value being used to control the comparing means; and
   M-ary counting means (70) for outputting a second count value by counting the carry pulse and the borrow pulse, the second count value being used to control the selecting means.

4. An interpolation pulse generating device according to any of the preceding claims wherein the difference signal generating means (500) generates a difference signal $\Delta S_j/n$ according to

$$\Delta S_j/n = (S_{j-1} - S_j)/n$$

   where n is a fixed integer.

5. An interpolation pulse generating device according to any of the preceding claims, wherein the device further comprises $k\Delta S_j/n$ generating means (600) for generating a signal $k\Delta S_j/n$ where k is an integer;

judgment signal generating means (700) for generating, based on the sinusoidal detection signal S_{j-1} and the signal $k\Delta S_j/n$, a judgement signal S_x according to

$$S_x = \{kS_j + (n - k)S_{j-1}\}/n;$$

and wherein the comparing means comprises first comparing means (800) for outputting a down-pulse P_- if the judgement signal S_x is smaller than 0; and
second comparing means (900) for outputting an up-pulse P_+ if the judgement signal S_x is larger than $\Delta S_j/n$.

6. An interpolation pulse generating device according to any of claims 1 to 4, wherein the device further comprises:

$k\Delta S_j/n$ generating means (600) for generating a signal $k\Delta S_j/n$ where k is an integer;
judgement signal generating means (700) for generating, based on the sinusoidal detection signal S_{j-1} and the signal $k\Delta S_j/n$, a judgement signal S_x according to

$$S_x = \{kS_j + (n - k)S_{j-1}\}/n;$$

and wherein the comparing means comprises first comparing means (800) for outputting a down-pulse P_- if the judgement signal S_x is smaller than $-\Delta S_j/n$; and
second comparing means (900) for outputting an up-pulse P_+ if the judgement signal S_x is larger than 0.

7. The interpolation pulse generating device according to claim 5 or claim 6, when dependent on at least claim 3, wherein the n-ary counting means (60) is adapted for decrementing the integer k by 1 when receiving the down-pulse P_- and, in the event that a decremented result is equal to 0, substituting n into k and outputting a borrow pulse, and for incrementing the integer k by 1 when receiving the up-pulse P_+ and, in the event that an incremented result is equal to n + 1, substituting 1 into k and outputting a carry pulse, a signal indicating the integer k being supplied to the $k\Delta S_j/n$ generating means; and wherein the
M-ary counting means (70) is adapted for decrementing the integer j by 1 when receiving the borrow pulse and, in the event that a decremented result is equal to 0, substituting M into j, and for incrementing the integer j by 1 when receiving the carry pulse and, in the event that an incremented result is equal to M + 1, substituting 1 into j, a signal indicating the integer j being supplied to the selecting means.

8. An interpolation pulse generating device that receives detection signals of a plurality of phases which signals are produced in accordance with a displacement of relative movement between corresponding members, and generates a count pulse for each predetermined phase-angle pitch that is smaller than one period of the detection signals, comprising:

selecting means (300) for receiving two sinusoidal detection signals that have the same amplitude, the same spatial period, and a predetermined spatial phase difference and that vary symmetrically with respect to a zero level, and for selecting, from M sinusoidal signals S_1-S_m deviating from each other at predetermined intervals, two adjacent sinusoidal signals S_j and S_{j-1} where an integer j = 1,2, ..., M, by combining the two sinusoidal detection signals;
difference signal generating means (520) for generating a difference signal Δ_{sj} according to

$$\Delta_{sj} = S_{j-1} - S_j$$

and an inverted difference signal $-\Delta_{sj}$;
A/D-converting means (1100) for A/D-converting the sinusoidal signal S_{j-1} using the signals ΔS_j and $-\Delta S_j$ as references; and,
comparing means (1200) for comparing an output A of an n-ary counting means and an output B of the A/D converting means, and for outputting an up-pulse P_+ if the output A is smaller than or equal to the output B, and outputting a down-pulse P_- if the output A is larger than the output B;

the n-ary counting means (61) for decrementing the integer k by 1 when receiving the down-pulse P_- and, in the event that a decremented result is smaller than 0, substituting n - 1 into k and outputting a borrow pulse, and for incrementing the integer k by 1 when receiving the up-pulse P_+ and, in the event that an incremented result is equal to n, substituting 0 into k and outputting a carry pulse, a signal indicating the integer k being supplied to the comparing means as the output A; and
M-ary counting means (70) for decrementing the integer j by 1 when receiving the borrow pulse and, in the event that a decremented result is equal to 0, substituting M into j, and for incrementing the integer j by 1 when receiving the carry pulse and, in the event that an incremented result is equal to M + 1, substituting 1 into j, a signal indicating the integer j being supplied to the selecting means.

9. The interpolation pulse generating device according to claim 8, further comprising a damper circuit for generating a count-up pulse only when the up-pulse P_+ is generated consecutively, and a count-down pulse only when the down-pulse P_- is generated consecutively, the count-up pulse and the count-down pulse being supplied to the comparing means instead of the up-pulse P_+ and the down-pulse P_-, respectively.

Patentansprüche

1. Vorrichtung zum Erzeugen von Interpolationsimpulsen, die Detektorsignale mit einer Vielzahl von Phasen empfängt, die in Übereinstimmung mit der relativen Bewegungsverschiebung zwischen entsprechenden Gliedern erzeugt werden, und einen Zählimpuls für jeden vorbestimmten Phasenwinkelabstand erzeugt, der kleiner ist als eine Periode der Detektorsignale, wobei die Vorrichtung umfasst:

   eine Auswahleinrichtung (300) zum Erzeugen von Signalen S_j und S_{j-1}, die voneinander um einen Phasenwert von $2\pi/M$ abweichen, indem die Vielzahl von Detektorsignalen kombiniert werden, wobei M eine festgelegte ganze Zahl ist,

   eine Differenzsignalerzeugungseinrichtung (500) zum Erzeugen einer Bezugssignals ΔS, das eine Differenz zwischen den Signalen S_j und S_{j-1} wiedergibt, und

   eine Vergleichseinrichtung (800) zum Erzeugen eines Aufwärtsimpulses oder eines Abwärtsimpulses, jedes Mal wenn das Signal S_j oder S_{j-1} um $\Delta S/n$ variiert, wobei n eine festgelegte ganze Zahl in einem Phasenabschnitt von $2\pi/M$ ist, in dem eines der Signale S_j und S_{j-1} einen positiven Wert und das andere Signal einen negativen Wert aufweist.

2. Vorrichtung zum Erzeugen von Interpolationsimpulsen nach Anspruch 1, wobei die Auswahleinrichtung (300) zwei sinusförmige Detektorsignale empfängt, die dieselbe Amplitude, dieselbe räumliche Periode und eine vorbestimmte räumliche Phasendifferenz aufweisen und symmetrisch in Bezug auf eine Nullebene variieren, und wobei die Auswahleinrichtung aus den M sinusförmigen Signalen S_1-S_M, die voneinander mit vorbestimmten Intervallen abweichen, wobei eine ganze Zahl J = 1, 2, ... M ist, die Signale S_j und S_{j-1} auswählt, indem sie die zwei sinusförmigen Detektorsignale kombiniert.

3. Vorrichtung zum Erzeugen von Interpolationsimpulsen nach Anspruch 1 oder Anspruch 2, die weiterhin umfasst:

   eine n-äre Zähleinrichtung (60) zum Ausgeben eines ersten Zählwerts und eines Übertrags- oder Borgeimpulses, indem sie die Aufwärtsimpulse und die Abwärtsimpulse zählt, wobei der erste Zählwert verwendet wird, um die Vergleichseinrichtung zu steuern, und

   eine M-äre Zähleinrichtung (70) zum Ausgeben eines zweiten Zählwerts, indem die Übertrags- und Borgeimpulse gezählt werden, wobei der zweite Zählwert verwendet wird, um die Auswahleinrichtung zu steuern.

4. Vorrichtung zum Erzeugen von Interpolationsimpulsen nach wenigstens einem der vorstehenden Ansprüche, wobei die Differenzsignalerzeugungseinrichtung (500) ein Differenzsignal $\Delta S_j/n$ in Übereinstimmung mit der folgenden Gleichung erzeugt:

$$\Delta S_j/n = (S_{j-1} - S_j)/n$$

wobei n eine festgelegte ganze Zahl ist.

5. Vorrichtung zum Erzeugen von Interpolationsimpulsen nach wenigstens einem der vorstehenden Ansprüche, wobei die Vorrichtung weiterhin umfasst:

eine $k\Delta S_j/n$-Erzeugungseinrichtung (600) zum Erzeugen eines Signals $k\Delta S_j/n$, wobei k eine ganze Zahl ist, und

eine Entscheidungssignalerzeugungseinrichtung (700), um auf der Basis des sinusförmigen Detektorsignals S_{j-1} und des Signals $k\Delta S_n/n$ ein Entscheidungssignal S_x in Übereinstimmung mit der folgenden Gleichung zu erzeugen:

$$S_x = \{kS_j + (n - k) S_{j-1}\} /n$$

und wobei die Vergleichseinrichtung umfasst:

eine erste Vergleichseinrichtung (800) zum Ausgeben eines Abwärtsimpulses P-, wenn das Entscheidungssignal S_x kleiner ist als 0, und

eine zweite Vergleichseinrichtung (900) zum Ausgeben eines Aufwärtsimpulses P+, wenn das Entscheidungssignal S_x größer ist als $\Delta S_j/n$.

6. Vorrichtung zum Erzeugen von Interpolationsimpulsen nach wenigstens einem der Ansprüche 1 bis 4, wobei die Vorrichtung weiterhin umfasst:

eine $k\Delta S_j/n$-Erzeugungseinrichtung (600) zum Erzeugen eines Signals $k\Delta S_j/n$, wobei k eine ganze Zahl ist,

eine Entscheidungssignalerzeugungseinrichtung (700), um auf der Basis des sinusförmigen Detektorsignals S_{j-1} und des Signals $k\Delta S_n/n$ ein Entscheidungssignal S_x in Übereinstimmung mit der folgenden Gleichung zu erzeugen:

$$S_x = \{kS_j + (n - k) S_{j-1}\}/n$$

und wobei die Vergleichseinrichtung umfasst:

eine erste Vergleichseinrichtung (800) zum Ausgeben eines Abwärtsimpulses P-, wenn das Entscheidungssignal S_x kleiner ist als $-\Delta S_j/n$, und

eine zweite Vergleichseinrichtung (900) zum Ausgeben eines Aufwärtsimpulses P+, wenn das Entscheidungssignal S_x größer ist als 0.

7. Vorrichtung zum Erzeugen von Interpolationsimpulsen nach Anspruch 5 oder 6 bei Abhängigkeit von wenigstens Anspruch 3, wobei die n-äre Zähleinrichtung (60) dafür ausgebildet ist, die ganze Zahl k um 1 zu dekrementieren, wenn der Abwärtsimpuls P-empfangen wird, und wenn das dekrementierte Ergebnis gleich 0 ist, n in k einzusetzen und einen Borgeimpuls auszugeben, sowie die ganze Zahl k um 1 zu inkrementieren, wenn der Aufwärtsimpuls P+ empfangen wird, und wenn das inkrementierte Ergebnis gleich n + 1 ist, 1 in k einzusetzen und einen Übertragimpuls auszugeben, um anzugeben, dass die ganze Zahl k an die $k\Delta S_j/n$-Erzeugungseinrichtung ausgegeben wird, und wobei die

M-äre Zähleinrichtung (70) dafür ausgebildet ist, die ganze Zahl j um 1 zu dekrementieren, wenn der Borgeimpuls empfangen wird, und wenn das dekrementierte Ergebnis gleich 0 ist, M in j einzusetzen, sowie die ganze Zahl j um 1 zu inkrementiere, wenn der Übertragimpuls empfangen wird, und wenn das inkrementierte Ergebnis gleich M + 1 ist, 1 in j einzusetzen, um anzugeben, dass die ganze Zahl j an die Auswahleinrichtung ausgegeben wird.

8. Vorrichtung zum Erzeugen von Interpolationsimpulsen, die Detektorsignale mit einer Vielzahl von Phasen empfängt, die in Übereinstimmung mit der relativen Bewegungsverschiebung zwischen entsprechenden Gliedern erzeugt werden, und einen Zählimpuls für jeden vorbestimmten Phasenwinkelabstand erzeugt, der kleiner ist als

eine Periode der Detektorsignale, wobei die Vorrichtung umfasst:

eine Auswahleinrichtung (300) zum Empfangen von zwei sinusförmigen Detektorsignalen, die dieselbe Amplitude, dieselbe räumliche Periode und eine vorbestimmte räumliche Phasendifferenz aufweisen und symmetrisch in Bezug auf eine Nullebene variieren, und zum Auswählen der Signale S_j und S_{j-1} aus den M sinusförmigen Signalen S_1-S_M, die durch voneinander durch vorbestimmte Intervalle abweichen, wobei eine ganze Zahl J = 1, 2, ... M ist, indem sie die zwei sinusförmigen Detektorsignale kombiniert,

eine Differenzsignalerzeugungseinrichtung (520) zum Erzeugen eines Differenzsignals Δ_{sj} in Übereinstimmung mit der folgenden Gleichung:

$$\Delta_{sj} = S_{j-1} - S_j$$

sowie eines umkehrten Differenzsignals $-\Delta_{sj}$,

eine A/D-Wandlereinrichtung (1100) zum A/D-Wandeln des sinusförmigen Signals S_{j-1} unter Verwendung der Signale ΔS_j und $-\Delta S_j$ als Bezugssignale,

eine Vergleichseinrichtung (1200) zum Vergleichen einer Ausgabe A einer n-ären Zähleinrichtung und einer Ausgabe B einer A/D-Wandlereinrichtung sowie zum Ausgeben eines Aufwärtsimpulses P+, wenn die Ausgabe A kleiner oder gleich der Ausgabe B ist, und zum Ausgeben eines Abwärtsimpulses P-, wenn die Ausgabe A größer ist als die Ausgabe B,

die n-äre Zähleinrichtung (61) zum Dekrementieren der ganzen Zahl j um 1, wenn der Abwärtsimpuls P- empfangen wird, und wenn das dekrementierte Ergebnis kleiner als 0 ist, zum Einsetzen von n - 1 in k und zum Ausgeben eines Borgeimpulses, sowie zum Inkrementieren der ganzen Zahl k um 1, wenn der Aufwärtsimpuls P+ empfangen wird, und wenn das inkrementierte Ergebnis gleich n ist, zum Einsetzen von 0 in k und zum Ausgeben eines Übertragsimpulses, um anzugeben, dass die ganze Zahl k als Ausgabe A an die Vergleichseinrichtung ausgegeben wird, und

eine M-äre Zähleinrichtung (70) zum Dekrementieren der ganzen Zahl j um 1, wenn der Borgeimpuls empfangen wird, und wenn das dekrementierte Ergebnis gleich 0 ist, zum Einsetzen von M in j, sowie zum Inkrementieren der ganzen Zahl j um 1, wenn der Übertragsimpuls empfangen wird, und wenn das inkrementierte Ergebnis gleich M + 1 ist, zum Einsetzen von 1 in j, um anzugeben, dass die ganze Zahl k zu der Auswahleinrichtung ausgegeben wird.

9. Vorrichtung zum Erzeugen von Interpolationsimpulsen nach Anspruch 8, die weiterhin eine Dämpfereinrichtung umfasst, um einen Count-Up-Impuls nur dann zu erzeugen, wenn der Aufwärtsimpuls P+ aufeinanderfolgend erzeugt wird, und um einen Count-Down-Impuls nur dann zu erzeugen, wenn der Abwärtsimpuls P- aufeinanderfolgend erzeugt wird, wobei der Count-Up-Impuls und der Count-Down-Impuls anstelle des Aufwärtsimpulses P+ und des Abwärtsimpulses P- jeweils an die Vergleichseinrichtung ausgegeben werden.

Revendications

1. Dispositif de génération d'impulsion d'interpolation qui reçoit des signaux de détection d'une pluralité de phases, lesquels signaux sont produits conformément à un déplacement de mouvement relatif entre des éléments se correspondant, et qui génère une impulsion de comptage pour chaque pas d'angle de phase prédéterminé qui est inférieur à une période des signaux de détection, comprenant :

un moyen de sélection (300) pour générer des signaux S_j et S_{j-1} qui sont déviés l'un par rapport à l'autre d'une valeur de phase de $2\pi/M$ en combinant la pluralité des signaux de détection, où M est un entier fixe ;
un moyen de génération de signal de différence (500) pour générer un signal de référence ΔS qui représente une différence entre les signaux S_j et S_{j-1} ; et
un moyen de comparaison (800, 900) pour générer une impulsion montante ou une impulsion descendante chaque fois que le signal S_j ou S_{j-1} varie de $\Delta S/n$ où n est un entier fixe dans une section de phase de $2\pi/M$ dans laquelle l'un des signaux S_j et S_{j-1} présente des valeurs positives et l'autre présente des valeurs néga-

tives.

2. Dispositif de génération d'impulsion d'interpolation selon la revendication 1, dans lequel le moyen de sélection (300) reçoit deux signaux de détection sinusoïdaux qui présentent la même amplitude, la même période spatiale et une différence de phase spatiale prédéterminée et qui varient de façon symétrique par rapport à un niveau de 0 et dans lequel le moyen de sélection sélectionne des signaux S_j et S_{j-1}, où un entier j = 1, 2, ..., M, parmi M signaux sinusoïdaux S_1 à S_M qui sont déviés les uns par rapport aux autres selon des intervalles prédéterminés, en combinant les deux signaux de détection sinusoïdaux.

3. Dispositif de génération d'impulsion d'interpolation selon la revendication 1 ou 2, comprenant en outre :

un moyen de comptage n-aire (60) pour émettre en sortie une première valeur de comptage et une impulsion de report ou de retenue en comptant l'impulsion montante et l'impulsion descendante, la première valeur de comptage étant utilisée pour commander le moyen de comparaison ; et
un moyen de comptage M-aire (70) pour émettre en sortie une seconde valeur de comptage en comptant l'impulsion de report et l'impulsion de retenue, la seconde valeur de comptage étant utilisée pour commander le moyen de sélection.

4. Dispositif de génération d'impulsion d'interpolation selon l'une quelconque des revendications précédentes, dans lequel le moyen de génération de signal de différence (500) génère un signal de différence $\Delta S_j/n$ conformément à :

$$\Delta S_j/n = (S_{j-1} - S_j)/n$$

où n est un entier fixe.

5. Dispositif de génération d'impulsion d'interpolation selon l'une quelconque des revendications précédentes, dans lequel le dispositif comprend en outre :

un moyen de génération de $k\Delta S_j/n$ (600) pour générer un signal $k\Delta S_j/n$ où k est un entier ;
un moyen de génération de signal d'appréciation (700) pour générer, sur la base du signal de détection sinusoïdal S_{j-1} et sur la base du signal $k\Delta S_j/n$, un signal d'appréciation S_x conformément à :

$$S_x = \{kS_j + (n - k)S_{j-1}\}/n \text{ ; et}$$

dans lequel le moyen de comparaison comprend :
un premier moyen de comparaison (800) pour émettre en sortie une impulsion descendante P- si le signal d'appréciation S_x est inférieur à 0 ; et
un second moyen de comparaison (900) pour émettre en sortie une impulsion montante P+ si le signal d'appréciation S_x est supérieur à $\Delta S_j/n$.

6. Dispositif de génération d'impulsion d'interpolation selon l'une quelconque des revendications 1 à 4, dans lequel le dispositif comprend en outre :

un moyen de génération de $k\Delta S_j/n$ (600) pour générer un signal $k\Delta S_j/n$ où k est un entier ;
un moyen de génération de signal d'appréciation (700) pour générer, sur la base du signal de détection sinusoïdal S_{j-1} et sur la base du signal $k\Delta S_j/n$, un signal d'appréciation S_x conformément à :

$$S_x = \{kS_j + (n - k)S_{j-1}\}/n \text{ ; et}$$

dans lequel le moyen de comparaison comprend :
un premier moyen de comparaison (800) pour émettre en sortie une impulsion descendante P- si le signal d'appréciation S_x est inférieur à $-\Delta S_j/n$; et
un second moyen de comparaison (900) pour émettre en sortie une impulsion montante P+ si le signal d'appréciation S_x est supérieur à 0.

7. Dispositif de génération d'impulsion d'interpolation selon la revendication 5 ou selon la revendication 6 lorsqu'elle dépend d'au moins la revendication 3, dans lequel le moyen de comptage n-aire (60) est adapté pour décrémenter l'entier k de 1 lors de la réception de l'impulsion de décomptage P- et, dans l'éventualité où un résultat décrémenté est égal à 0, pour substituer n dans k et pour émettre en sortie une impulsion de retenue, et pour incrémenter l'entier k de 1 lors de la réception de impulsion montante P+ et, dans l'éventualité où un résultat incrémenté est égal à n + 1, pour substituer 1 dans k et pour émettre en sortie une impulsion de report, un signal indiquant l'entier k étant appliqué sur le moyen de génération de $k\Delta S_j/n$; et

dans lequel :

le moyen de comptage M-aire (70) est adapté pour décrémenter l'entier j de 1 lors de la réception de l'impulsion de retenue et, dans l'éventualité où un résultat décrémenté est égal à 0, pour substituer M dans j, et pour incrémenter l'entier j de 1 lors de la réception de l'impulsion de report et, dans l'éventualité où un résultat incrémenté est égal à M + 1, pour substituer 1 dans j, un signal indiquant l'entier j étant appliqué sur le moyen de sélection.

8. Dispositif de génération d'impulsion d'interpolation qui reçoit des signaux de détection d'une pluralité de phases, lesquels signaux sont produits conformément à un déplacement de mouvement relatif entre des éléments se correspondant, et qui génère une impulsion de comptage pour chaque pas d'angle de phase prédéterminé qui est inférieur à une période des signaux de détection, comprenant :

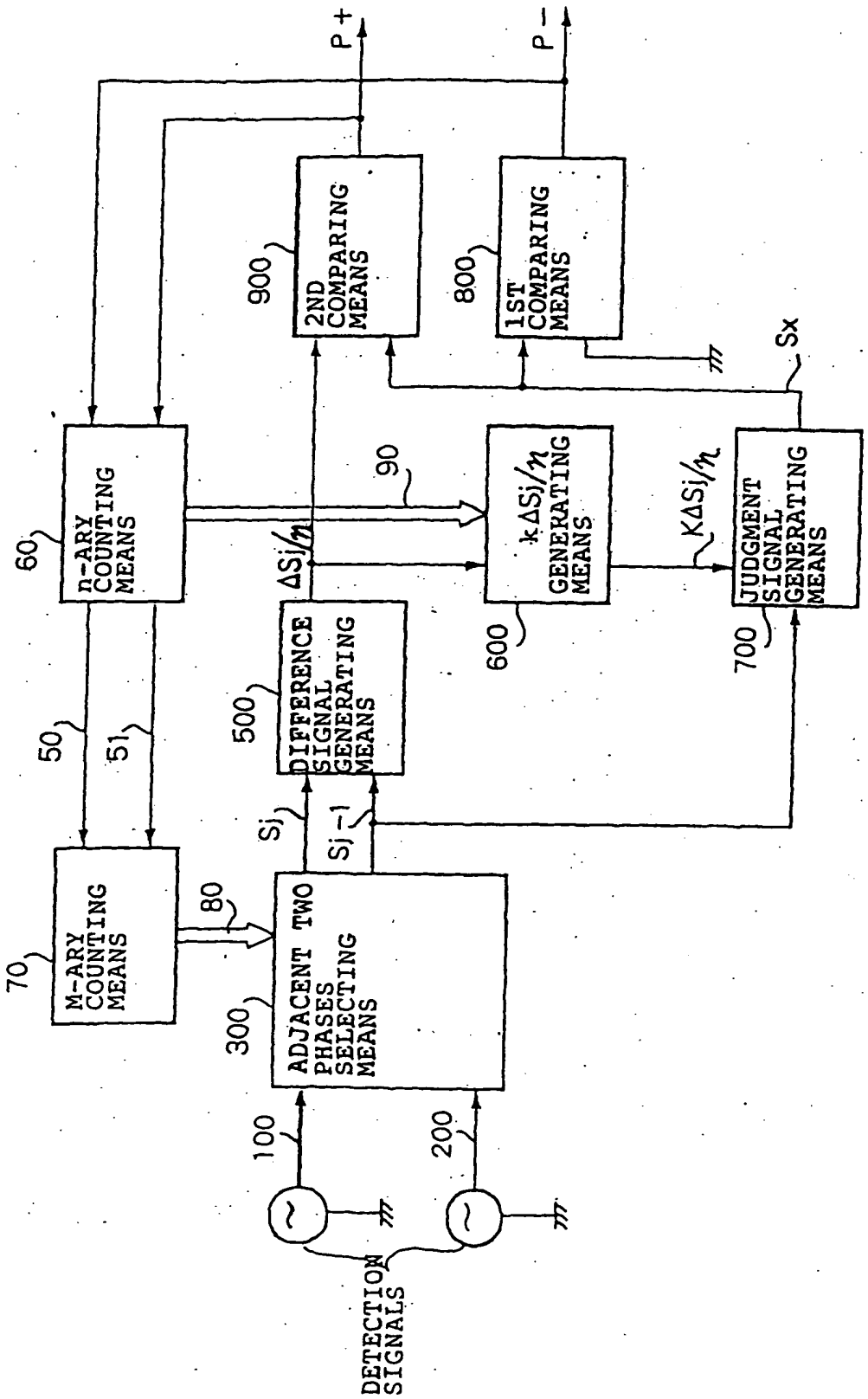
un moyen de sélection (300) pour recevoir deux signaux de détection sinusoïdaux qui présentent la même amplitude, la même période spatiale et une différence de phase spatiale prédéterminée et qui varient de façon symétrique par rapport à un niveau de 0 et pour sélectionner, parmi M signaux sinusoïdaux S_1 à S_M qui sont déviés les uns par rapport aux autres selon des intervalles prédéterminés, deux signaux sinusoïdaux adjacents S_j et S_{j-1} où un entier j = 1, 2, ..., M, en combinant les deux signaux de détection sinusoïdaux ;
un moyen de génération de signal de différence (520) pour générer un signal de différence ΔS_j conformément à

$$\Delta S_j = S_{j-1} - S_j$$

et un signal de différence inversé $-\Delta S_j$;
un moyen de conversion A/N (1100) pour convertir A/N le signal sinusoïdal S_{j-1} en utilisant les signaux ΔS_j et $-\Delta S_j$ en tant que références ; et
un moyen de comparaison (1200) pour comparer une sortie A d'un moyen de comptage n-aire et une sortie B du moyen de conversion A/N et pour émettre en sortie une impulsion montante P+ si la sortie A est inférieure ou égale à la sortie B et pour émettre en sortie une impulsion descendante P- si la sortie A est supérieure à la sortie B ;
le moyen de comptage n-aire (61) pour décrémenter l'entier k de 1 lors de la réception de l'impulsion descendante P- et, dans l'éventualité où un résultat décrémenté est inférieur à 0, pour substituer n - 1 dans k et pour émettre en sortie une impulsion de retenue et pour incrémenter l'entier k de 1 lors de la réception de l'impulsion montante P+ et, dans l'éventualité où un résultat incrémenté est égal à n, pour substituer 0 dans k et pour émettre en sortie une impulsion de report, un signal indiquant l'entier k étant appliqué sur le moyen de comparaison en tant que sortie A ; et
un moyen de comptage M-aire (70) pour décrémenter l'entier j de 1 lors de la réception de l'impulsion de retenue et, dans l'éventualité où un résultat décrémenté est égal à 0, pour substituer M dans j et pour incrémenter l'entier j de 1 lors de la réception de l'impulsion de report et, dans l'éventualité où un résultat incrémenté est égal à M + 1, pour substituer 1 dans j, un signal indiquant l'entier j étant appliqué sur le moyen de sélection.

9. Dispositif de génération d'impulsion d'interpolation selon la revendication 8, comprenant en outre un circuit d'amortisseur pour générer une impulsion de comptage seulement lorsque l'impulsion montante P+ est générée de façon consécutive et une impulsion de décomptage seulement lorsque l'impulsion descendante P- est générée de façon consécutive, l'impulsion de comptage et l'impulsion de décomptage étant appliquées sur le moyen de comparaison en lieu et place respectivement de l'impulsion montante P+ et de l'impulsion descendante P-.

Fig. 1


P+
P−
900
2ND COMPARING MEANS
800
1ST COMPARING MEANS
Sx
60
n-ARY COUNTING MEANS
90
k·ΔSj/n
GENERATING MEANS
KΔSj/n
JUDGMENT SIGNAL GENERATING MEANS
ΔSj/n
600
700
500
DIFFERENCE SIGNAL GENERATING MEANS
50
51
Sj
Sj −1
70
M-ARY COUNTING MEANS
80
300
ADJACENT TWO PHASES SELECTING MEANS
100
200
DETECTION SIGNALS

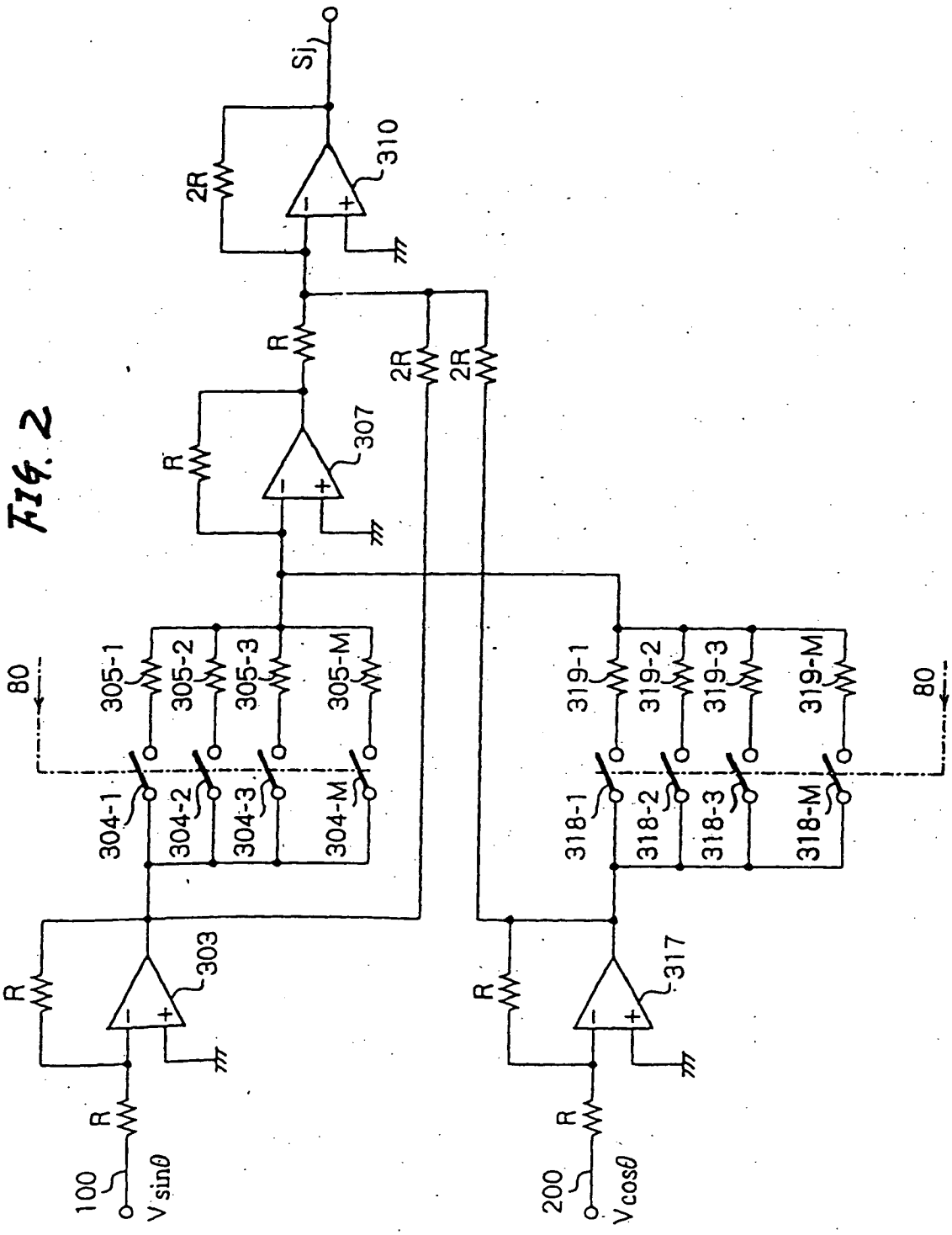

Sj
310
2R
R
307
2R
2R
R
80
305-1
305-2
305-3
305-M
304-1
304-2
304-3
304-M
319-1
319-2
319-3
319-M
318-1
318-2
318-3
318-M
80
303
317
R
R
R
R
100
V sinθ
200
V cosθ

Fig. 2

FIG. 3

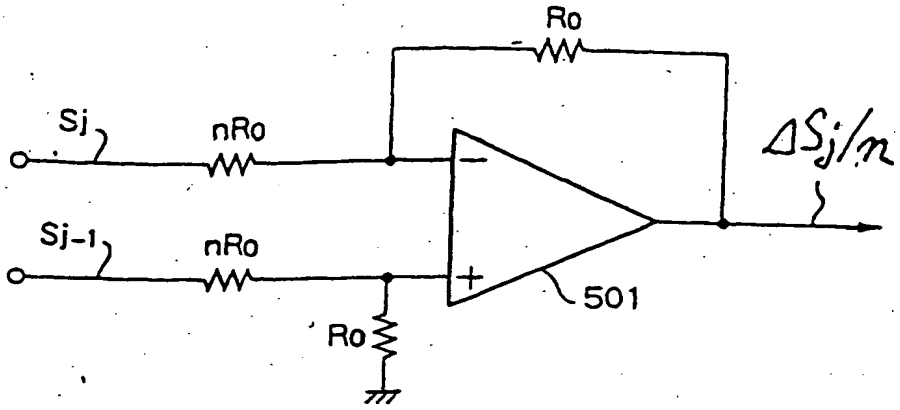

Ro
Sj
nRo
ΔSj/n
Sj-1
nRo
501
Ro

FIG. 4

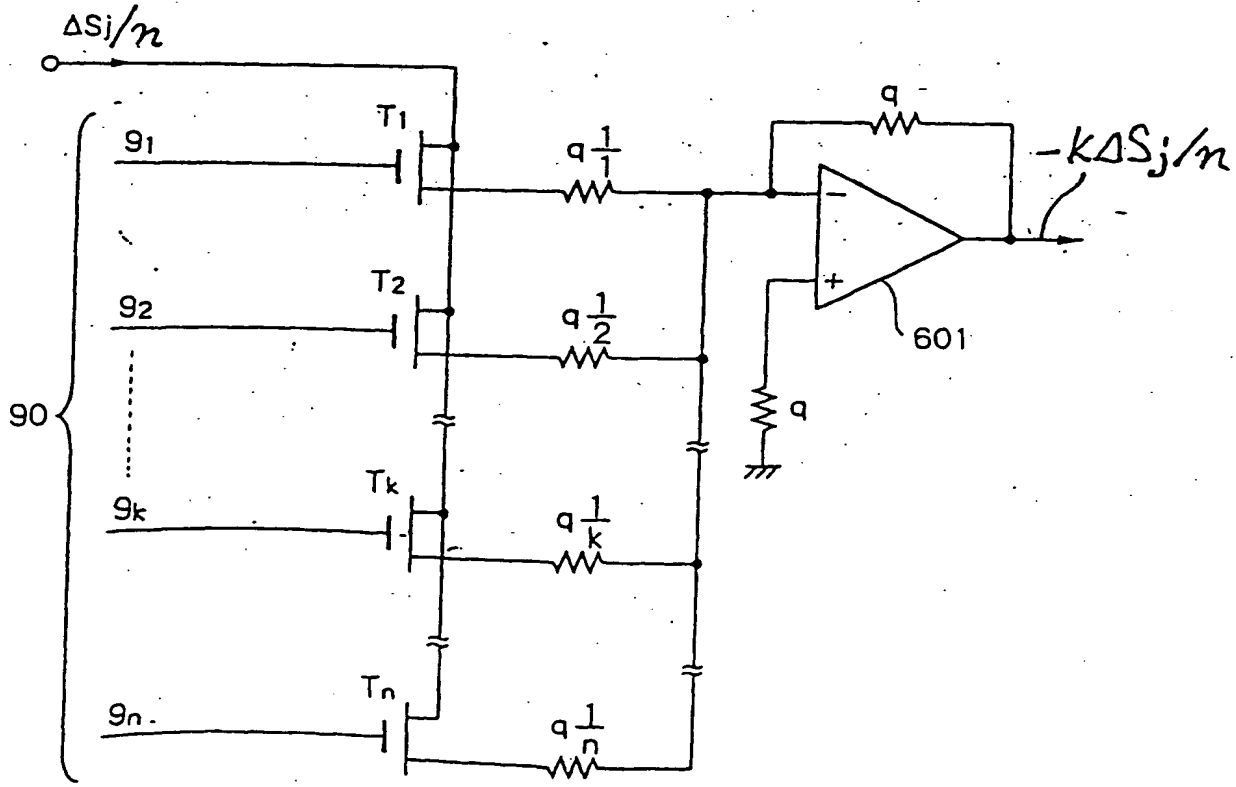

ΔSj/n
T1
g1
q 1/1
q
-kΔSj/n
T2
g2
q 1/2
601
90
q
Tk
gk
q 1/k
Tn
gn
q 1/n

FIG. 5

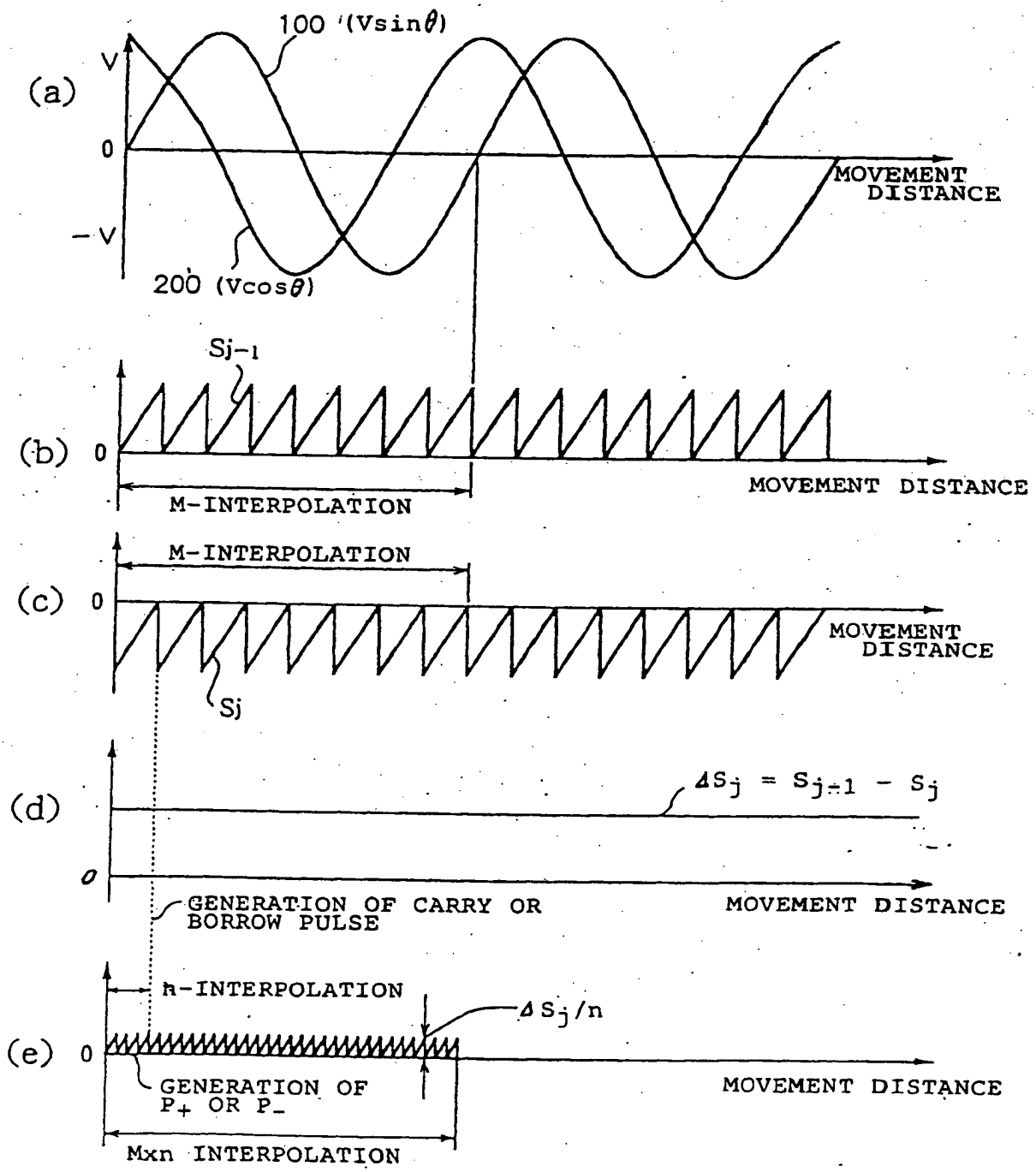

(a)
100 (Vsinθ)
V
0
-V
200 (Vcosθ)
MOVEMENT DISTANCE
(b)
Sj-1
0
M-INTERPOLATION
MOVEMENT DISTANCE
(c)
M-INTERPOLATION
0
Sj
MOVEMENT DISTANCE
(d)
ΔSj = Sj+1 - Sj
0
GENERATION OF CARRY OR BORROW PULSE
MOVEMENT DISTANCE
n-INTERPOLATION
ΔSj/n
(e)
0
GENERATION OF P+ OR P-
MOVEMENT DISTANCE
Mxn INTERPOLATION

FIG. 6

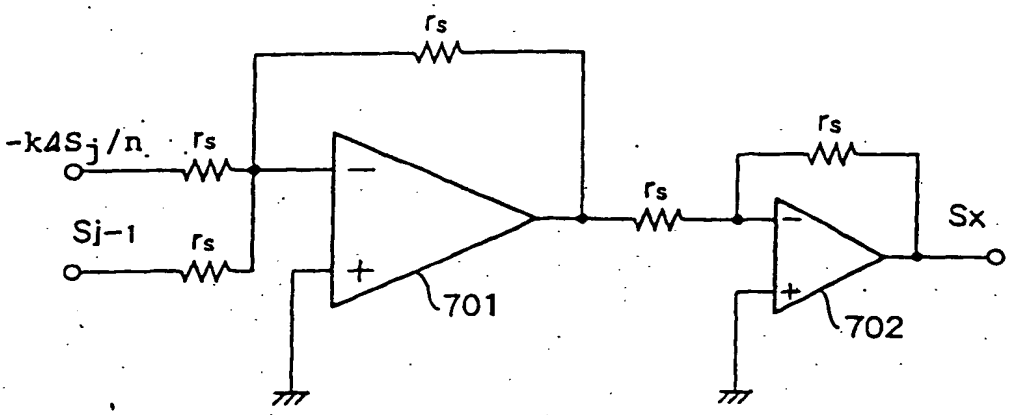

rs
-kΔSj/n
rs
Sj-1
rs
701
rs
rs
Sx
702

FIG. 7

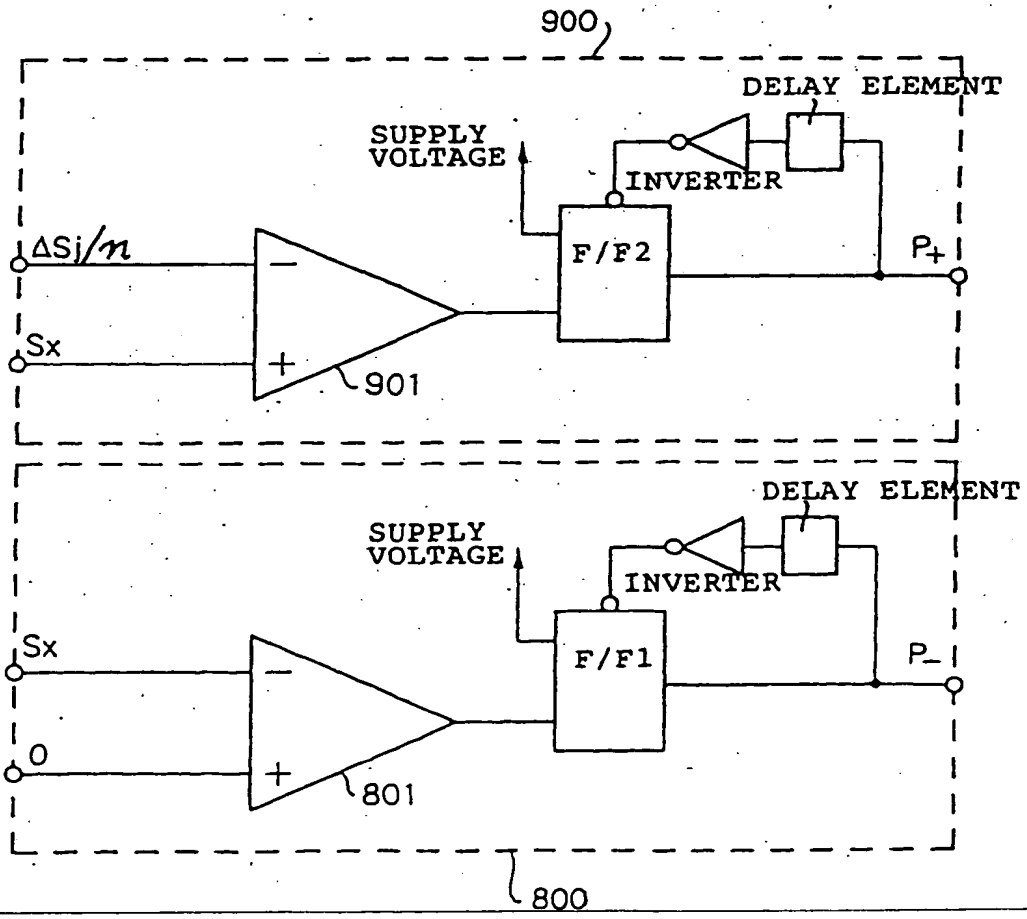

900
DELAY ELEMENT
SUPPLY VOLTAGE
INVERTER
ΔSj/n
F/F2
P+
Sx
901
DELAY ELEMENT
SUPPLY VOLTAGE
INVERTER
Sx
F/F1
P-
0
801
800

FIG. 8 PRIOR ART

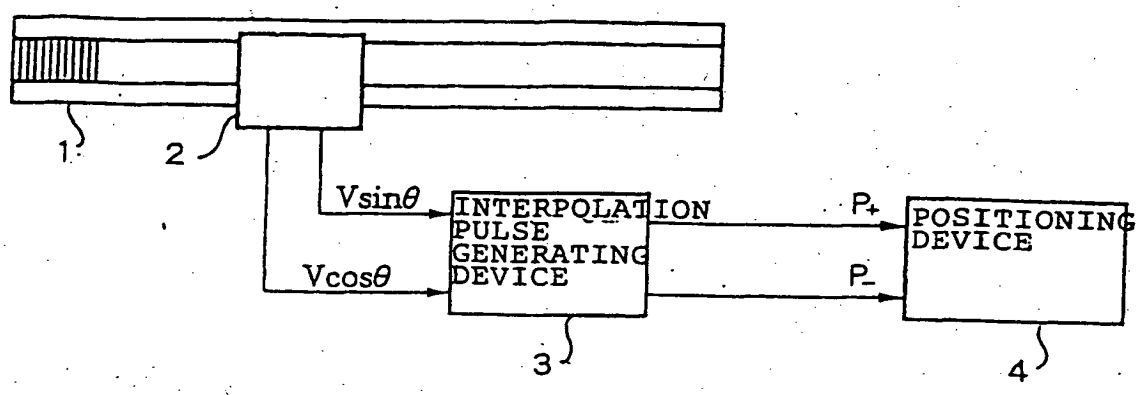
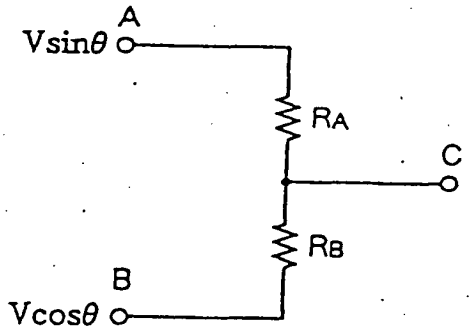


FIG. 9 PRIOR ART



$$C=\frac{V\sqrt{R_A^2+R_B^2}}{R_A+R_B}\sin(\theta+\phi)$$

WHERE $\phi=\tan^{-1}\frac{R_A}{R_B}$

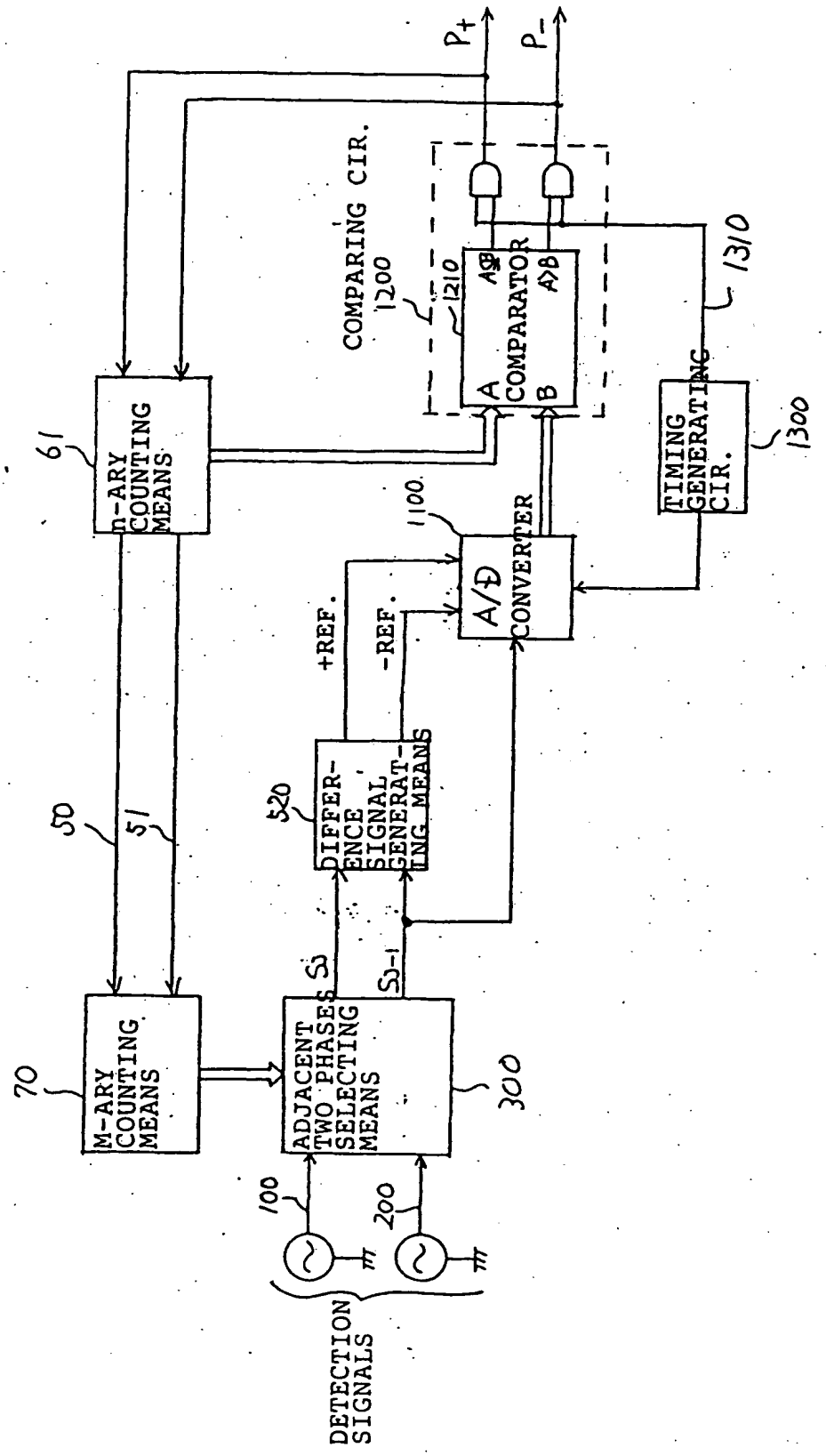
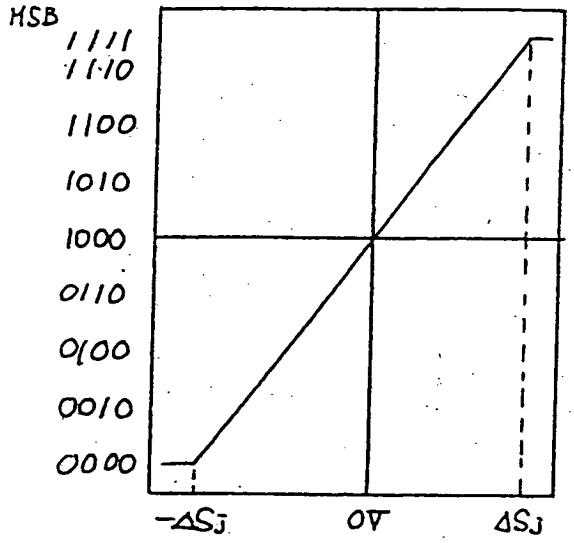

P+
P-
COMPARING CIR.
1200
1210
A≧B
A<B
COMPARATOR
A
B
1310
TIMING GENERATING CIR.
1300
61
n-ARY COUNTING MEANS
1100
A/D CONVERTER
+REF.
-REF.
50
51
52
DIFFER-ENCE SIGNAL GENERAT-ING MEANS
53
53-1
70
M-ARY COUNTING MEANS
ADJACENT TWO PHASES SELECTING MEANS
300
100
200
DETECTION SIGNALS

FIG. 10

FIG. 11



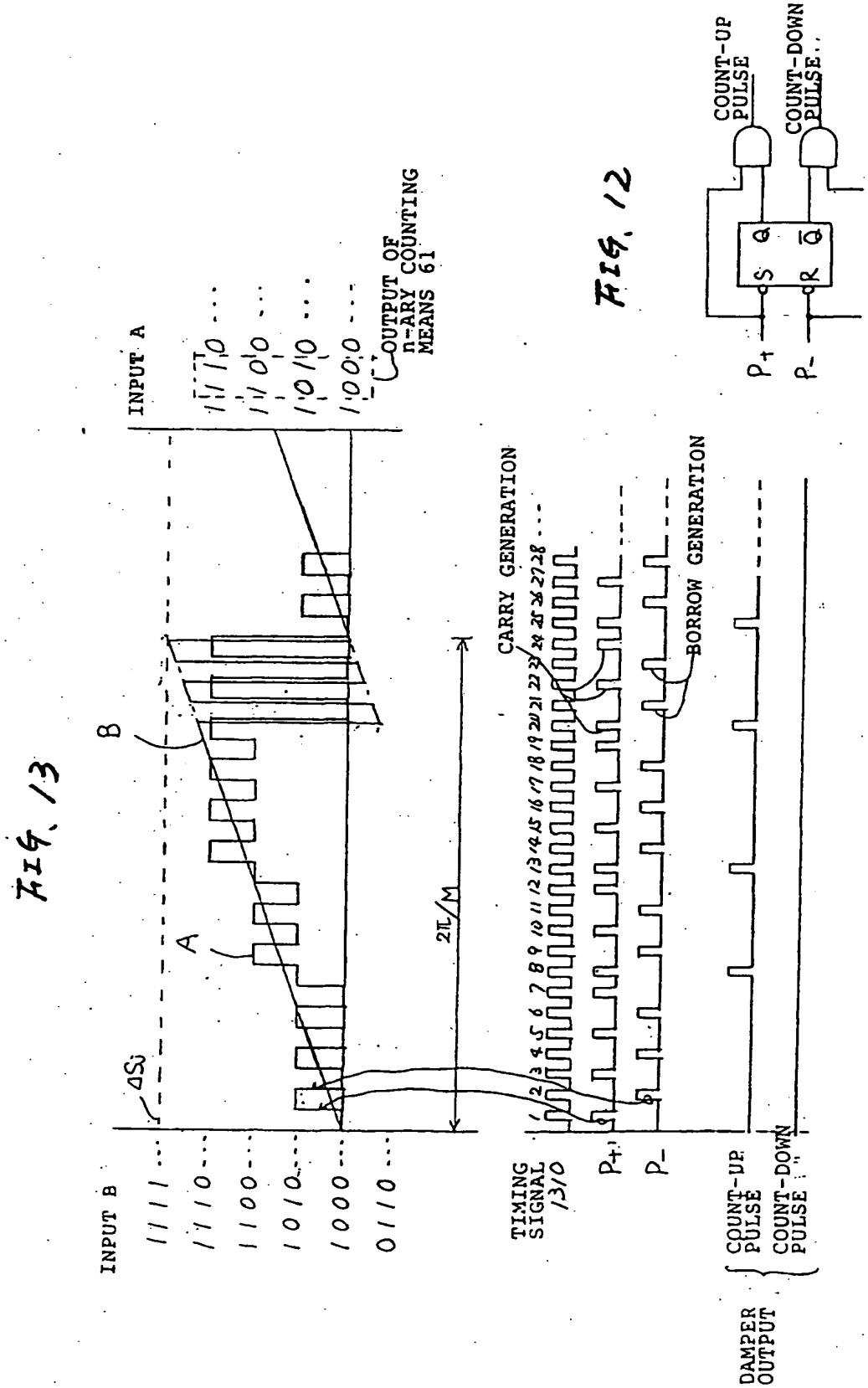
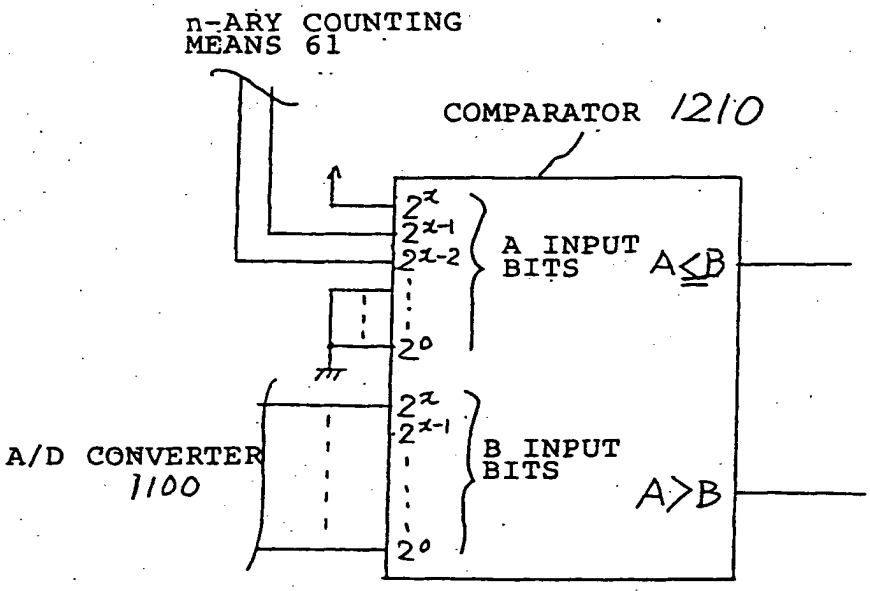

INPUT A
1111 ...
1110 ...
1010 ...
1000 ...
OUTPUT OF n-ARY COUNTING MEANS 61
B
A
ΔS
2π/M
INPUT B
1111 ...
1110 ...
1100 ...
1010 ...
1000 ...
0110 ...
CARRY GENERATION
BORROW GENERATION
TIMING SIGNAL 13/0
P+
P-
COUNT-UP PULSE
COUNT-DOWN PULSE
DAMPER OUTPUT
COUNT-UP PULSE
COUNT-DOWN PULSE
S
R
Q
Q̄
P+
P-

Fig. 13

Fig. 12

FIG. 14


n-ARY COUNTING MEANS 61
COMPARATOR 1210
2^x
2^{x-1}
2^{x-2}
2^0
A INPUT BITS
A≤B
2^x
2^{x-1}
2^0
B INPUT BITS
A>B
A/D CONVERTER 1100